RF3146

MICRO•DEVICES

QUAD-BAND GSM850/GSM900/DCS/PCS POWER AMP MODULE

Part of the POLARIS™ TOTAL RADIO™ Solution

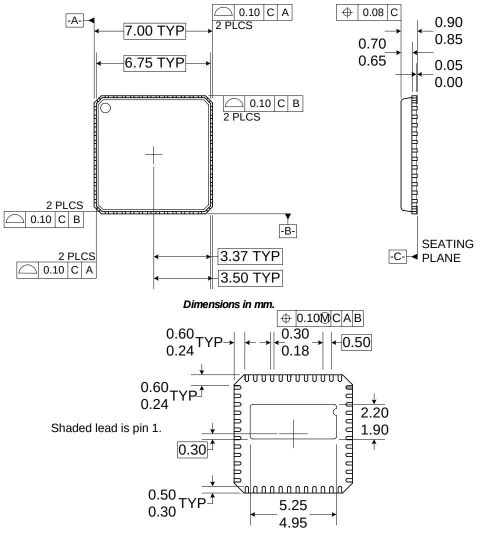
Typical Applications

- 3V Quad-Band GSM Handsets
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- GSM850/EGSM900/DCS/PCS Products
- GPRS Class 12 Compatible
- Power Star™ Module

Product Description

The RF3146 is a high-power, high-efficiency power amplifier module with integrated power control. The device is a self-contained 7mmx7mmx0.9mm lead frame module (LFM) with 50Ω input and output terminals. The power control function is also incorporated, eliminating the need for directional couplers, detector diodes, power control ASICs and other power control circuitry; this allows the module to be driven directly from the DAC output. The device is designed for use as the final RF amplifier in GSM850, EGSM900, DCS and PCS handheld digital cellular equipment and other applications in the 824MHz to 849MHz, 880MHz to 915MHz, 1710MHz to 1785MHz and 1850MHz to 1910MHz bands. On-board power control provides over 50dB of control range with an analog voltage input; and, power down with a logic "low" for standby operation.

The RF3146 is part of the POLARIS™ TOTAL RADIO™ solution.



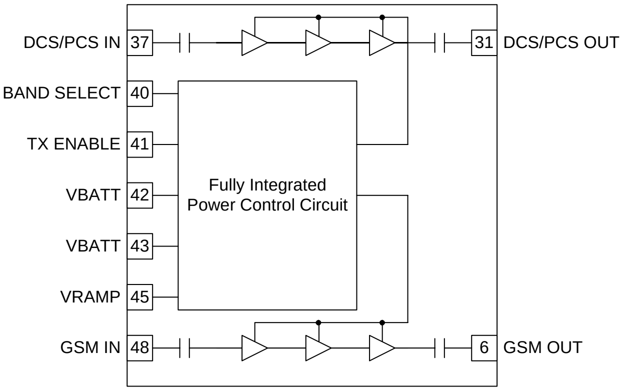
Package Style: LFM, 48-Pin, 7mmx7mmx0.9mm

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☑ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS

Features

- Integrated V_{REG}
- Complete Power Control Solution
- +35dBm GSM Output Power at 3.5V
- +33dBm DCS/PCS Output Power at 3.5V
- 60% GSM and 55% DCS/PCS $_{EFF}$
- 7mmx7mmx0.9mm Package Size



Functional Block Diagram

Ordering Information

RF3146	Quad-Band GSM850/GSM900/DCS/PCS Power Amp Module
RF3146P	Quad-Band GSM850/GSM900/DCS/PCS Power Amp Module (Pb Free)
RF3146 SB	Power Amp Module 5-Piece Sample Pack
RF3146 PCBA	Fully Assembled Evaluation Board

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RF3146

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.3 to +6.0	V_{DC}
Power Control Voltage (V_{RAMP})	-0.3 to +1.8	V
Input RF Power	+10	dBm
Max Duty Cycle	50	%
Output Load VSWR	10:1	
Operating Case Temperature	-20 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall Power Control					
V_{RAMP}					
Power Control “ON”			1.5	V	Max. P_{OUT}, Voltage supplied to the input
Power Control “OFF”		0.2	0.25	V	Min. P_{OUT}, Voltage supplied to the input
V_{RAMP} Input Capacitance		15	20	pF	DC to 2MHz
V_{RAMP} Input Current			10	µA	$V_{RAMP}=V_{RAMP\ MAX}$
Turn On/Off Time			2	µs	V_{RAMP}=0.2V to $V_{RAMP\ MAX}$
TX Enable “ON”	1.5			V	
TX Enable “OFF”			0.5	V	
GSM Band Enable			0.5	V	
DCS/PCS Band Enable	1.9			V	
Overall Power Supply					
Power Supply Voltage	3.0	3.5	5.5	V	Specifications
				V	Nominal operating limits
Power Supply Current		1		µA	P_{IN}<-30dBm, TX Enable=Low, Temp=-20°C to +85°C
				mA	V_{RAMP}=0.2V, TX Enable=High
Overall Control Signals					
Band Select “Low”	0	0	0.5	V	
Band Select “High”	1.9	2.0	3.0	V	
Band Select “High” Current		20	50	µA	
TX Enable “Low”	0	0	0.5	V	
TX Enable “High”	1.5	2.0	3.0	V	
TX Enable “High” Current		1	2	µA	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (GSM850 Mode)					Temp=+25°C, V_{BATT}=3.5V, V_{RAMP}=$V_{RAMP\ MAX}$, P_{IN}=3dBm, Freq=824MHz to 849MHz, 25% Duty Cycle, Pulse Width=1154µs
Operating Frequency Range		824 to 849		MHz	
Maximum Output Power	+34.2			dBm	Temp = 25°C, V_{BATT}=3.5V, V_{RAMP}=$V_{RAMP\ MAX}$
	+32.0			dBm	Temp=+85°C, V_{BATT}=3.0V, V_{RAMP}=$V_{RAMP\ MAX}$
Total Efficiency	47	55		%	At $P_{OUT\ MAX}$, V_{BATT}=3.5V
Input Power Range	0	+3	+5	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power		-88	-81	dBm	RBW=100kHz, 869MHz to 894MHz, $P_{OUT}\geq$ +5dBm
Forward Isolation 1		-50	-35	dBm	TXEnable=Low, P_{IN}=+5dBm
Forward Isolation 2		-35	-15	dBm	TXEnable=High, P_{IN}=+5dBm, V_{RAMP}=0.2V
Cross Band Isolation at $2f_0$			-18	dBm	V_{RAMP}=0.2V to V_{RAMP}_R_P
Second Harmonic		-15	-7	dBm	V_{RAMP}=0.2V to V_{RAMP}_R_P
Third Harmonic		-25	-15	dBm	V_{RAMP}=0.2V to V_{RAMP}_R_P
All Other Non-Harmonic Spurious			-36	dBm	V_{RAMP}=0.2V to $V_{RAMP\ MAX}$
Input Impedance		50		Ω	
Input VSWR			2.5:1		V_{RAMP}=0.2V to $V_{RAMP\ MAX}$
Output Load VSWR Stability	8:1				Spurious<-36dBm, RBW=3MHz Set V_{RAMP} where $P_{OUT}\leq$34.2dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V_{RAMP} where $P_{OUT}\leq$34.2dBm into 50Ω load. No damage or permanent degradation to part.
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range		55		dB	V_{RAMP}=0.2V to $V_{RAMP\ MAX}$

Notes:

$V_{RAMP\ MAX}$=0.4*V_{BATT}+0.06≤1.5V

V_{RAMP}_R_P=V_{RAMP} set for 34.2dBm at nominal conditions.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (GSM900 Mode)					Temp=+25°C, V_{BATT}=3.5V, V_{RAMP}=$V_{RAMP\ MAX}$, P_{IN}=3dBm, Freq=880MHz to 915MHz, 25% Duty Cycle, Pulse Width=1154µs
Operating Frequency Range		880 to 915		MHz	
Maximum Output Power	+34.2			dBm	Temp = 25°C, V_{BATT}=3.5V, V_{RAMP}=$V_{RAMP\ MAX}$
	+32.0			dBm	Temp=+85°C, V_{BATT}=3.0V, V_{RAMP} =$V_{RAMP\ MAX}$
Total Efficiency	54	58		%	At $P_{OUT\ MAX}$, V_{BATT}=3.5V
Input Power Range	0	+3	+5	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power		-86	-80	dBm	RBW=100kHz, 925MHz to 935MHz, $P_{OUT} \geq$ +5dBm
		-88	-84	dBm	RBW=100kHz, 935MHz to 960MHz, $P_{OUT} \geq$ +5dBm
Forward Isolation 1		-45	-35	dBm	TXEnable=Low, P_{IN}=+5dBm
Forward Isolation 2		-30	-15	dBm	TXEnable=High, V_{RAMP}=0.2V, P_{IN}=+5dBm
Cross Band Isolation 2f_0			-17	dBm	V_{RAMP}=0.2V to $V_{RAMP_}R_P$
Second Harmonic		-15	-10	dBm	V_{RAMP}=0.2V to $V_{RAMP_}R_P$
Third Harmonic		-25	-15	dBm	V_{RAMP}=0.2V to $V_{RAMP_}R_P$
All Other Non-Harmonic Spurious			-36	dBm	V_{RAMP}=0.2V to $V_{RAMP\ MAX}$
Input Impedance		50		Ω	
Input VSWR			2.5:1		V_{RAMP}=0.2V to $V_{RAMP\ MAX}$
Output Load VSWR Stability	8:1				Spurious<-36dBm, RBW=3MHz Set V_{RAMP} where $P_{OUT} \leq$34.2dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V_{RAMP} where $P_{OUT} \leq$34.2dBm into 50Ω load. No damage or permanent degradation to part.
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range		50		dB	V_{RAMP}=0.2V to $V_{RAMP\ MAX}$

Notes:

$V_{RAMP\ MAX}$=0.4*V_{BATT}+0.06≤1.5V

$V_{RAMP_}R_P$=V_{RAMP} set for 34.2dBm at nominal conditions.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (DCS Mode)					Temp=25°C, V_{BATT}=3.5V, V_{RAMP}=$V_{RAMP\ MAX}$, P_{IN}=3dBm, Freq=1710MHz to 1785MHz, 25% Duty Cycle, pulse width=1154µs
Operating Frequency Range		1710 to 1785		MHz	
Maximum Output Power	+32.0			dBm	Temp=25°C, V_{BATT}=3.5V, V_{RAMP} =$V_{RAMP\ MAX}$
	30			dBm	Temp=+85°C, V_{BATT}=3.0V, V_{RAMP}=$V_{RAMP\ MAX}$
Total Efficiency	45	52		%	At $P_{OUT\ MAX}$, V_{BATT}=3.5V
Input Power Range	0	+3	+5	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power		-85	-80	dBm	RBW=100kHz, 1805MHz to 1880MHz, $P_{OUT} \geq$ 0dBm, V_{BATT}=3.5V
Forward Isolation 1		-50	-35	dBm	TXEnable=Low, P_{IN}=+5dBm
Forward Isolation 2		-25	-15	dBm	TXEnable=High, V_{RAMP}=0.2V, P_{IN}=+5dBm
Second Harmonic		-15	-7	dBm	V_{RAMP}=0.2V to V_{RAMP}_R_P
Third Harmonic		-20	-15	dBm	V_{RAMP}=0.2V to V_{RAMP}_R_P
All Other Non-Harmonic Spurious			-36	dBm	V_{RAMP}=0.2V to $V_{RAMP\ MAX}$
Input Impedance		50		Ω	
Input VSWR			2.5:1		V_{RAMP}=0.2V to $V_{RAMP\ MAX}$
Output Load VSWR Stability	8:1				Spurious<-36dBm, RBW=3MHz Set V_{RAMP} where $P_{OUT} \leq$32.0dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V_{RAMP} where $P_{OUT} \leq$32.0dBm into 50Ω load. No damage or permanent degradation to part.
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pin
Power Control V_{RAMP}					
Power Control Range		50		dB	V_{RAMP}=0.2V to $V_{RAMP\ MAX}$, P_{IN}=+5dBm

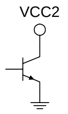
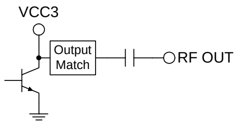
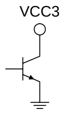
Notes:

$V_{RAMP\ MAX}$=0.4*V_{BATT}+0.06≤1.5V

V_{RAMP}_R_P=V_{RAMP} set for 32.0dBm at nominal conditions.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (PCS Mode)					Temp=25°C, V_{BATT}=3.5V, V_{RAMP} =$V_{RAMP\ MAX}$, P_{IN}=3dBm, Freq=1850MHz to 1910MHz, 25% Duty Cycle, pulse width=1154μs
Operating Frequency Range		1850 to 1910		MHz	
Maximum Output Power	+32.0			dBm	Temp=25°C, V_{BATT}=3.5V, V_{RAMP}=$V_{RAMP\ MAX}$, 1850MHz to 1910MHz
	30			dBm	Temp=+85°C, V_{BATT}=3.0V, V_{RAMP}=$V_{RAMP\ MAX}$
Total Efficiency	48	55		%	At $P_{OUT\ MAX}$, V_{BATT}=3.5V
Input Power Range	0	+3	+5	dBm	Full output power guaranteed at minimum drive level
Output Noise Power		-85	-80	dBm	RBW=100kHz, 1930MHz to 1990MHz, P_{OUT} ≥ 0dBm, V_{BATT}=3.5V
Forward Isolation 1		-40	-33	dBm	TX_ENABLE=Low, P_{IN}=+5dBm
Forward Isolation 2		-20	-15	dBm	TXEnable=High, V_{RAMP}=0.2V, P_{IN}=+5dBm
Second Harmonic		-15	-7	dBm	V_{RAMP}=0.2V to V_{RAMP}_R_P
Third Harmonic		-20	-15	dBm	V_{RAMP}=0.2V to V_{RAMP}_R_P
All Other Non-Harmonic Spurious			-36	dBm	V_{RAMP}=0.2V to $V_{RAMP\ MAX}$
Input Impedance		50		Ω	
Input VSWR			2.5:1		V_{RAMP}=0.2V to $V_{RAMP\ MAX}$
Output Load VSWR Stability	8:1				Spurious<-36dBm, RBW=3MHz Set V_{RAMP} where P_{OUT}≤32.0dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V_{RAMP} where P_{OUT}≤32.0dBm into 50Ω load. No damage or permanent degradation to part.
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pin
Power Control V_{RAMP}					
Power Control Range		50		dB	V_{RAMP}=0.2V to $V_{RAMP\ MAX}$, P_{IN}=+5dBm

Notes:
$V_{RAMP\ MAX}$=0.4*V_{BATT}+0.06≤1.5V
V_{RAMP}_R_P=V_{RAMP} set for 32.0dBm at nominal conditions.

Pin	Function	Description	Interface Schematic
1	NC	Internal circuit node. Do not externally connect.	
2	VCC2 GSM	Controlled voltage input to the GSM driver stage. This voltage is part of the power control function for the module. This node must be connected to VCC OUT. This pin should be externally decoupled.	
3	NC	Internal circuit node. Do not externally connect.	
4	GND	Internally connected to the package base.	
5	GND	Internally connected to the package base.	
6	GSM850/ GSM900 OUT	RF output for the GSM bands. This is a 50Ω output. The output matching circuit and DC-block are internal to the package.	
7	GND	Internally connected to the package base.	
8	NC	Internal circuit node. Do not externally connect.	
9	NC	Internal circuit node. Do not externally connect.	
10	NC	Internal circuit node. Do not externally connect.	
11	NC	Internal circuit node. Do not externally connect.	
12	NC	Internal circuit node. Do not externally connect.	
13	NC	No internal or external connection.	
14	NC	Internal circuit node. Do not externally connect.	
15	NC	Internal circuit node. Do not externally connect.	
16	NC	Internal circuit node. Do not externally connect.	
17	NC	Internal circuit node. Do not externally connect.	
18	VCC3 GSM	Controlled voltage input to the GSM output stage. This voltage is part of the power control function for the module. This node must be connected to VCC OUT. This pin should be externally decoupled.	
19	VCC OUT	Controlled voltage output to feed VCC2 and VCC3. This voltage is part of the power control function for the module. It cannot be connected to any pins other than VCC2 and VCC3.	
20	VCC OUT	Controlled voltage output to feed VCC2 and VCC3. This voltage is part of the power control function for the module. It cannot be connected to any pins other than VCC2 and VCC3.	
21	VCC3 DCS/PCS	Controlled voltage input to the DCS/PCS output stage. This voltage is part of the power control function for the module. This node must be connected to VCC OUT. This pin should be externally decoupled.	See pin 18.
22	NC	Internal circuit node. Do not externally connect.	
23	NC	Internal circuit node. Do not externally connect.	
24	NC	No internal or external connection.	
25	NC	Internal circuit node. Do not externally connect.	
26	NC	Internal circuit node. Do not externally connect.	
27	NC	Internal circuit node. Do not externally connect.	
28	NC	Internal circuit node. Do not externally connect.	
29	NC	Internal circuit node. Do not externally connect.	
30	GND	Internally connected to the package base.	

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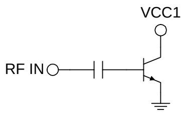
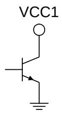
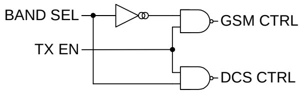
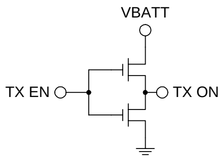
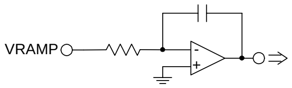
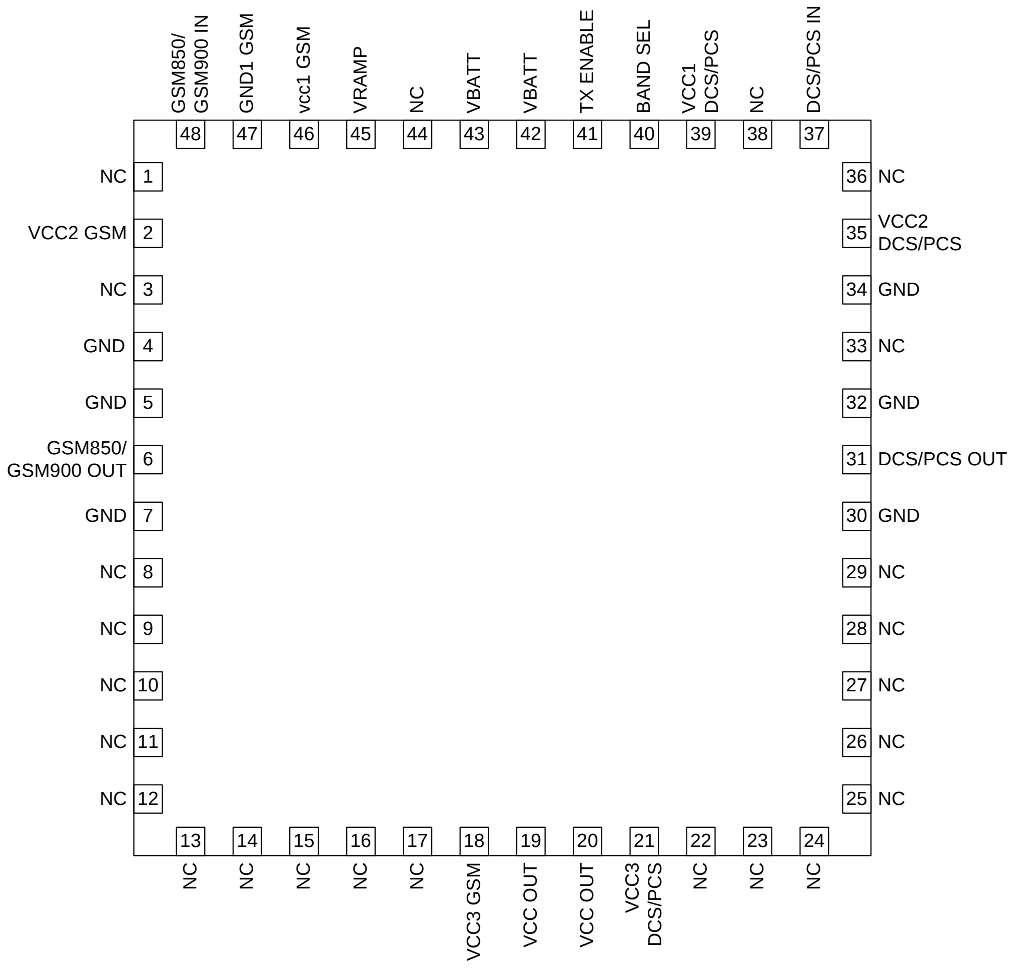
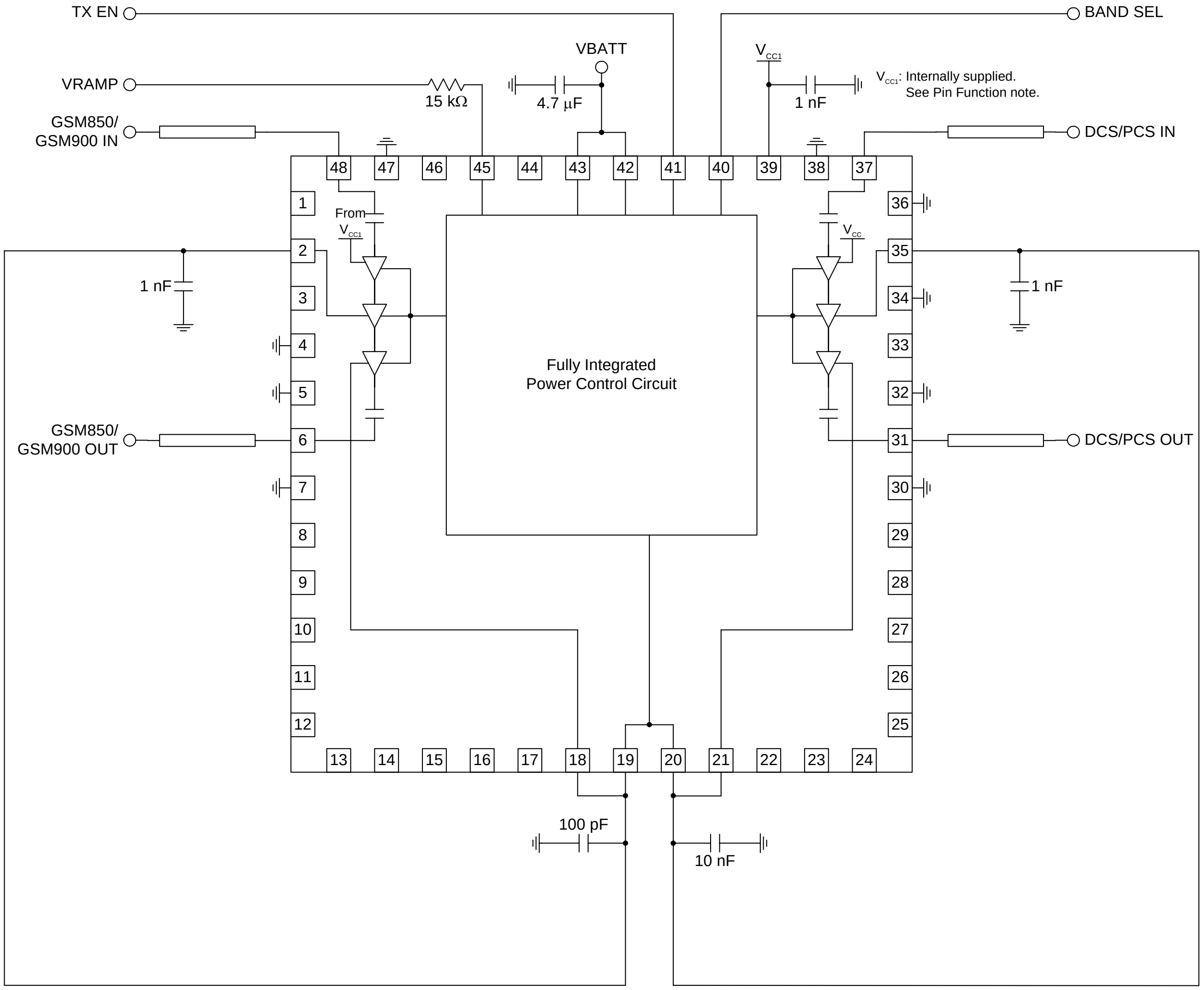
Pin	Function	Description	Interface Schematic
31	**DCS/PCS OUT**	RF output for the DCS/PCS bands. This is a 50Ω output. The output matching circuit and DC-block are internal to the package.	See pin 6.
32	**GND**	Internally connected to the package base.	
33	**NC**	Internal circuit node. Do not externally connect.	
34	**GND**	Internally connected to the package base.	
35	**VCC2 DCS/PCS**	Controlled voltage input to the DCS/PCS driver stage. This voltage is part of the power control function for the module. This node must be connected to VCC OUT. This pin should be externally decoupled.	See pin 2.
36	**NC**	No internal connection. Connect to ground plane close to the package pin.	
37	**DCS/PCS IN**	RF input to the DCS/PCS band. This is a 50Ω output.	
38	**NC**	No internal connection. Connect to ground plane close to the package pin.	
39	**VCC1 DCS/PCS**	Controlled voltage on the GSM and DCS/PCS preamplifier stages. This voltage is applied internal to the package. This pin should be externally decoupled.	
40	**BAND SEL**	Allows external control to select the GSM or DCS/PCS bands with a logic high or low. A logic low enables the GSM bands, whereas a logic high enables the DCS/PCS bands.	
41	**TX ENABLE**	This signal enables the PA module for operation with a logic high. Both bands are disabled with a logic low.	
42	**VBATT**	Power supply for the module. This pin should be externally decoupled and connected to the battery.	
43	**VBATT**	Power supply for the module. This pin should be externally decoupled and connected to the battery.	
44	**NC**	Internal circuit node. Do not externally connect.	
45	**VRAMP**	Ramping signal from DAC. A simple RC filter may be required depending on the selected baseband.	
46	**VCC1 GSM**	Internally connected to VCC1 (pin 39). No external connection required.	See pin 39.
47	**GND1 GSM**	Ground connection for the GSM preamplifier stage. Connect to ground plane close to the package pin.	
48	**GSM850/ GSM900 IN**	RF input to the GSM band. This is a 50Ω input.	See pin 37.
Pkg Base	**GND**	Connect to ground plane with multiple via holes. See recommended footprint.	

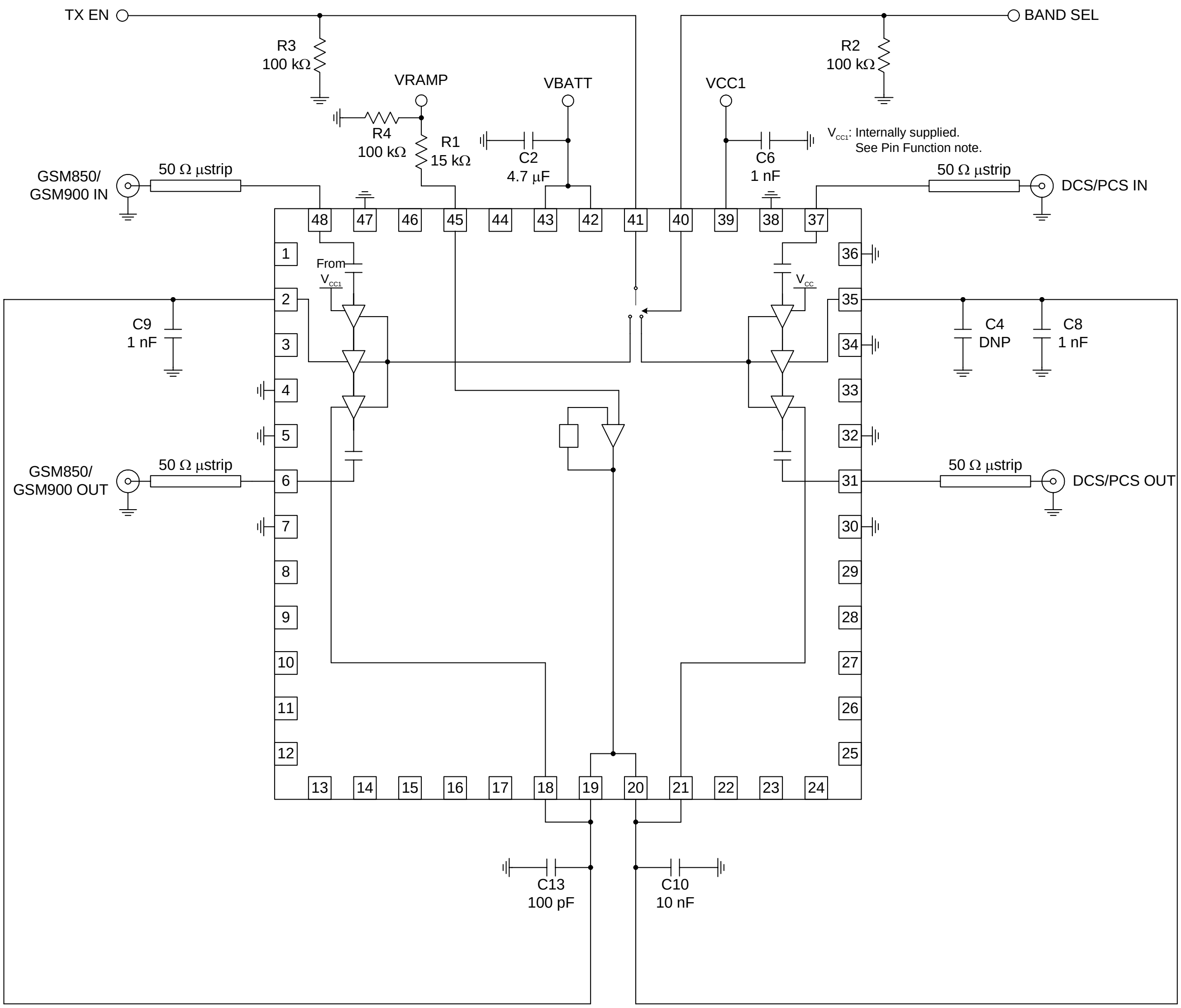
Pin Out


GSM850/ GSM900 IN
48
GND1 GSM
47
vcc1 GSM
46
VRAMP
45
NC
44
VBATT
43
VBATT
42
TX ENABLE
41
BAND SEL
40
VCC1 DCS/PCS
39
NC
38
DCS/PCS IN
37
NC
1
VCC2 GSM
2
NC
3
GND
4
GND
5
GSM850/ GSM900 OUT
6
GND
7
NC
8
NC
9
NC
10
NC
11
NC
12
36
NC
35
VCC2 DCS/PCS
34
GND
33
NC
32
GND
31
DCS/PCS OUT
30
GND
29
NC
28
NC
27
NC
26
NC
25
NC
13
NC
14
NC
15
NC
16
NC
17
NC
18
VCC3 GSM
19
VCC OUT
20
VCC OUT
21
VCC3 DCS/PCS
22
NC
23
NC
24
NC

Application Schematic

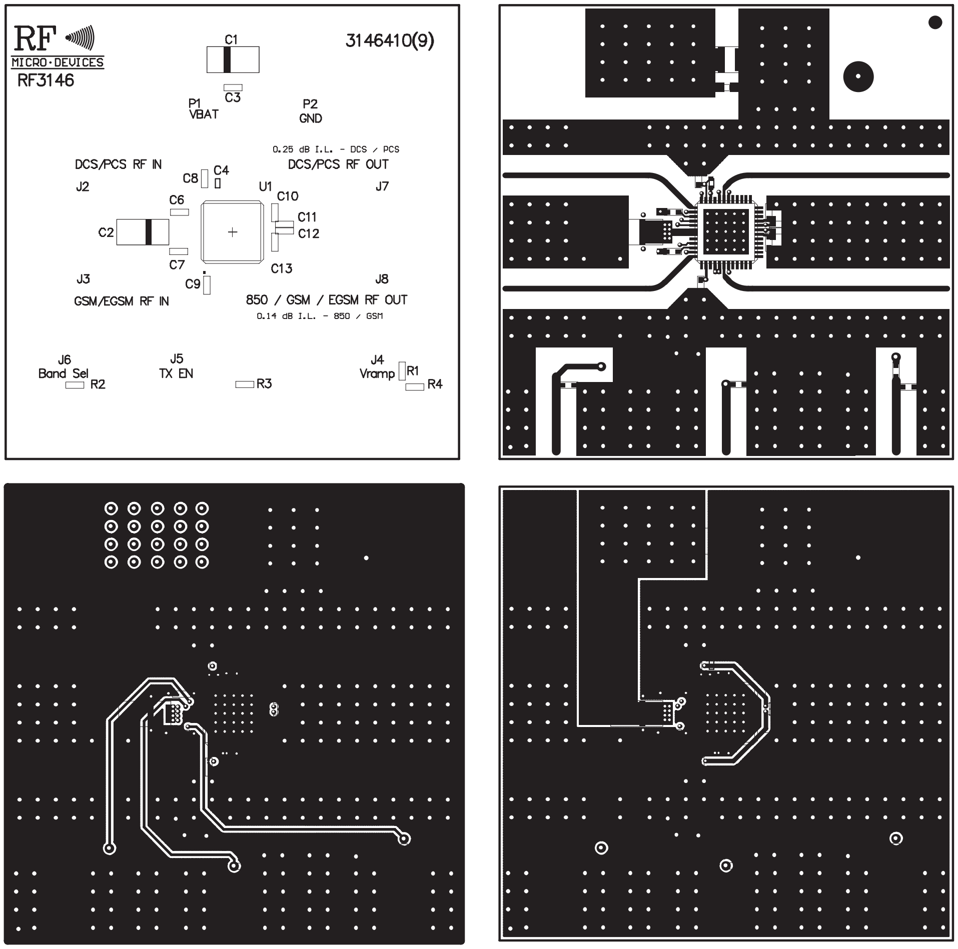


Evaluation Board Schematic



Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.032”, Board Material FR-4, Multi-Layer



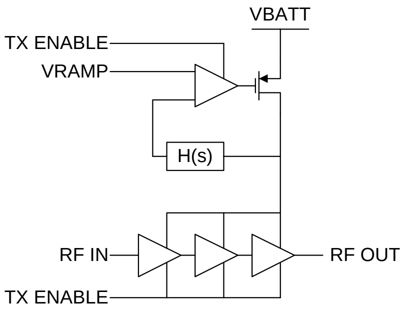
Theory of Operation

Overview

The RF3146 is a quad-band GSM850, EGSM900, DCS1800, and PCS1900 power amplifier module that incorporates an indirect closed loop method of power control. This simplifies the phone design by eliminating the need for the complicated control loop design. The indirect closed loop appears as an open loop to the user and can be driven directly from the DAC output in the baseband circuit.

Theory of Operation

The indirect closed loop is essentially a closed loop method of power control that is invisible to the user. Most power control systems in GSM sense either forward power or collector/drain current. The RF3146 does not use a power detector. A high-speed control loop is incorporated to regulate the collector voltage of the amplifier while the stage are held at a constant bias. The V_{RAMP} signal is multiplied by a factor of 2.65 and the collector voltage for the second and third stages are regulated to the multiplied V_{RAMP} voltage. The basic circuit is shown in the following diagram.



By regulating the power, the stages are held in saturation across all power levels. As the required output power is decreased from full power down to 0dBm, the collector voltage is also decreased. This regulation of output power is demonstrated in Equation 1 where the relationship between collector voltage and output power is shown. Although load impedance affects output power, supply fluctuations are the dominate mode of power variations. With the RF3146 regulating collector voltage, the dominant mode of power fluctuations is eliminated.

$$P_{dBm} = 10 \cdot \log\left[\frac{(2 \cdot V_{CC} - V_{SAT})^2}{8 \cdot R_{LOAD} \cdot 10^{-3}}\right] \qquad \text{(Eq. 1)}$$

There are several key factors to consider in the implementation of a transmitter solution for a mobile phone. Some of them are:

- Current draw and system efficiency
- Power variation due to Supply Voltage
- Power variation due to frequency
- Power variation due to temperature
- Input impedance variation
- Noise power
- Loop stability
- Loop bandwidth variations across power levels
- Burst timing and transient spectrum trade offs
- Harmonics

Output power does not vary due to supply voltage under normal operating conditions if V_{RAMP} is sufficiently lower than V_{BATT}. By regulating the collector voltage to the PA the voltage sensitivity is essentially eliminated. This covers most cases where the PA will be operated. However, as the battery discharges and approaches its lower power range the maximum output power from the PA will also drop slightly. In this case it is important to also decrease V_{RAMP} to prevent the power control from inducing switching transients. These transients occur as a result of the control loop slowing down and not regulating power in accordance with V_{RAMP}.

The switching transients due to low battery conditions are regulated by incorporating the following relationship limiting the maximum V_{RAMP} voltage (Equation 2). Although no compensation is required for typical battery conditions, the battery compensation required for extreme conditions is covered by the relationship in Equation 4. This should be added to the terminal software.

$$V_{RAMPMAX} = 0.4 \cdot V_{BATT} + 0.06 \leq 1.5V \quad \text{(Eq. 2)}$$

Due to reactive output matches, there are output power variations across frequency. There are a number of components that can make the effects greater or less.

The components following the power amplifier often have insertion loss variation with respect to frequency. Usually, there is some length of microstrip that follows the power amplifier. There is also a frequency response found in directional couplers due to variation in the coupling factor over frequency, as well as the sensitivity of the detector diode. Since the RF3146 does not use a directional coupler with a diode detector, these variations do not occur.

Input impedance variation is found in most GSM power amplifiers. This is due to a device phenomena where C_{BE} and C_{CB} (C_{GS} and C_{SG} for a FET) vary over the bias voltage. The same principle used to make varactors is present in the power amplifiers. The junction capacitance is a function of the bias across the junction. This produces input impedance variations as the Vapc voltage is swept. Although this could present a problem with frequency pulling the transmit VCO off frequency, most synthesizer designers use very wide loop bandwidths to quickly compensate for frequency variations due to the load variations presented to the VCO.

The RF3146 presents a very constant load to the VCO. This is because all stages of the RF3146 are run at constant bias. As a result, there is constant reactance at the base emitter and base collector junction of the input stage to the power amplifier.

Noise power in PA's where output power is controlled by changing the bias voltage is often a problem when backing off of output power. The reason is that the gain is changed in all stages and according to the noise formula (Equation 5),

$$F_{TOT} = F1 + \frac{F2 - 1}{G1} + \frac{F3 - 1}{G1 \cdot G2} \quad \text{(Eq. 3)}$$

the noise figure depends on noise factor and gain in all stages. Because the bias point of the RF3146 is kept constant the gain in the first stage is always high and the overall noise power is not increased when decreasing output power.

Power control loop stability often presents many challenges to transmitter design. Designing a proper power control loop involves trade-offs affecting stability, transient spectrum and burst timing.

In conventional architectures the PA gain (dB/ V) varies across different power levels, and as a result the loop bandwidth also varies. With some power amplifiers it is possible for the PA gain (control slope) to change from 100dB/V to as high as 1000dB/V. The challenge in this scenario is keeping the loop bandwidth wide enough to meet the burst mask at low slope regions which often causes instability at high slope regions.

The RF3146 loop bandwidth is determined by internal bandwidth and the RF output load and does not change with respect to power levels. This makes it easier to maintain loop stability with a high bandwidth loop since the bias voltage and collector voltage do not vary.

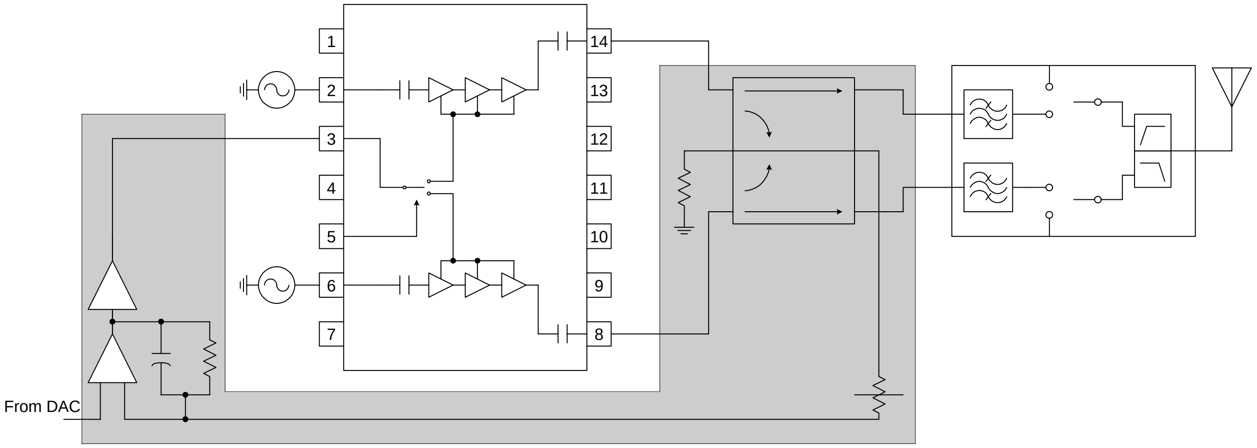
An often overlooked problem in PA control loops is that a delay not only decreases loop stability it also affects the burst timing when, for instance the input power from the VCO decreases (or increases) with respect to temperature or supply voltage. The burst timing then appears to shift to the right especially at low power levels. The RF3146 is insensitive to a change in input power and the burst timing is constant and requires no software compensation.

Switching transients occur when the up and down ramp of the burst is not smooth enough or suddenly changes shape. If the control slope of a PA has an inflection point within the output power range or if the slope is simply too steep it is difficult to prevent switching transients. Controlling the output power by changing the collector voltage is as earlier described based on the physical relationship between voltage swing and output power. Furthermore all stages are kept constantly biased so inflection points are nonexistent.

Harmonics are natural products of high efficiency power amplifier design. An ideal class "E" saturated power amplifier will produce a perfect square wave. Looking at the Fourier transform of a square wave reveals high harmonic content. Although this is common to all power amplifiers, there are other factors that contribute to conducted harmonic content as well. With most power control methods a peak power diode detector is used to rectify and sense forward power. Through the rectification process there is additional squaring of the waveform resulting in higher harmonics. The RF3146 address this by eliminating the need for the detector diode. Therefore the harmonics coming out of the PA should represent the maximum power of the harmonics throughout the transmit chain. This is based upon proper harmonic termination of the transmit port. The receive port termination on the T/R switch as well as the harmonic impedance from the switch itself will have an impact on harmonics. Should a problem arise, these terminations should be explored.

The RF3146 incorporates many circuits that had previously been required external to the power amplifier. The shaded area of the diagram below illustrates those components and the following table itemizes a comparison between the RF3146 Bill of Materials and a conventional solution.

Component	Conventional Solution	RF3146
Power Control ASIC	$0.80	N/A
Directional Coupler	$0.20	N/A
Buffer	$0.05	N/A
Attenuator	$0.05	N/A
Various Passives	$0.05	N/A
Mounting Yield (other than PA)	$0.12	N/A
Total	**$1.27**	**$0.00**



*Shaded area eliminated with Indirect Closed Loop using RF3146

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

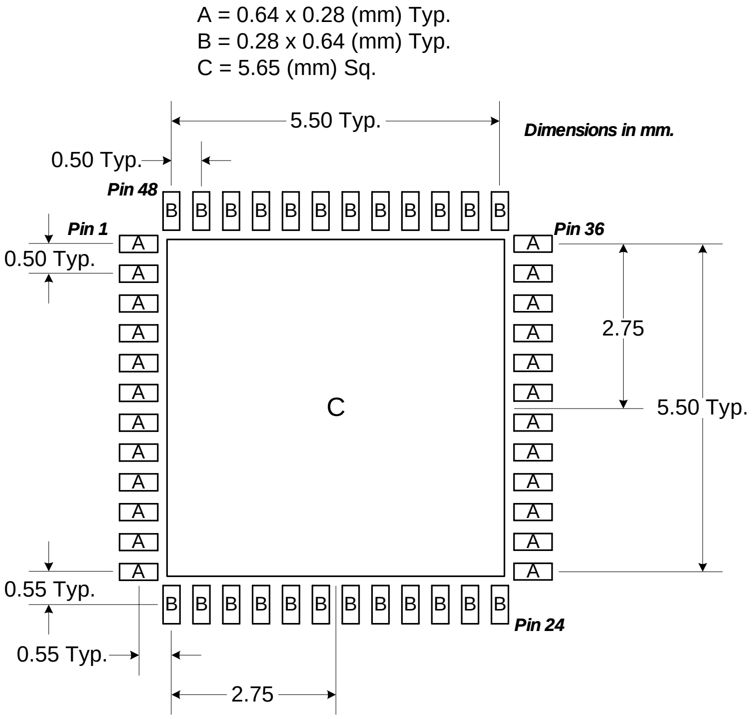


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

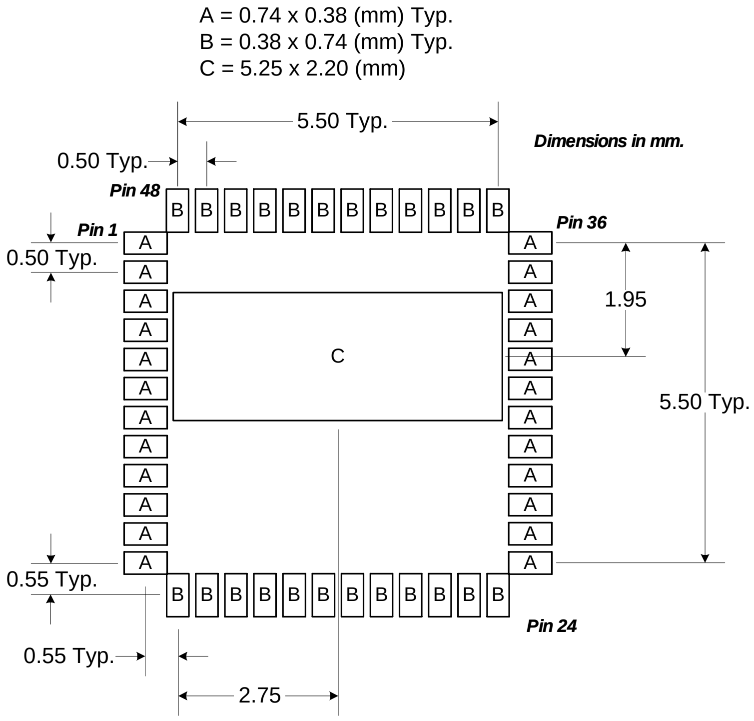


Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.